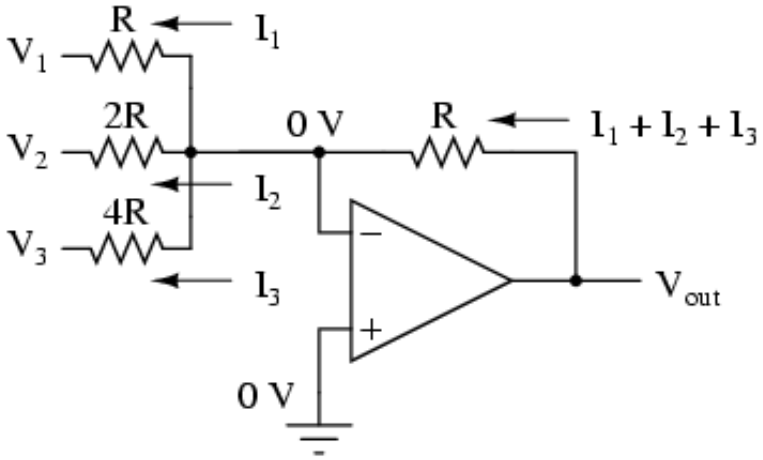
Digital to Analogue Converters (DAC)

A Digital to Analogue Converters (DAC) can be constructed using :

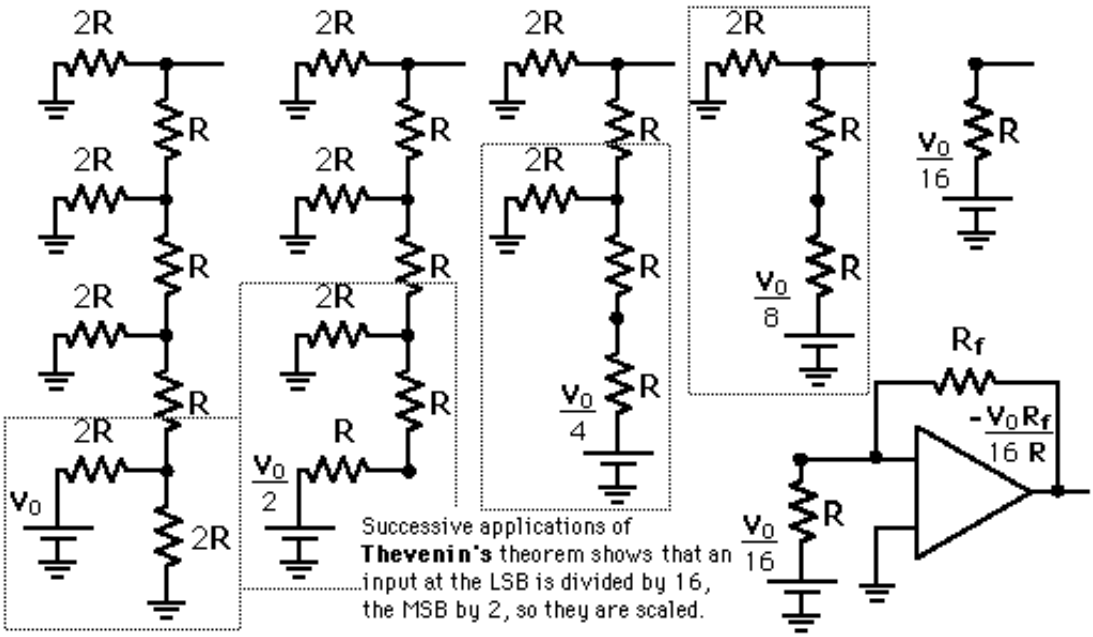
1) A Binary Weighted Ladder:



$$V_{out} = -\left(V_1 + \frac{V_2}{2} + \frac{V_3}{4}\right)$$

Starting from V_1 and going through V_3, this would give each input voltage exactly half the effect on the output as the voltage before it. In other words, input voltage V_1 has a 1:1 effect on the output voltage (gain of 1), while input voltage V_2 has half that much effect on the output (a gain of 1/2), and V_3 half of that (a gain of 1/4). These ratios are the same ratios corresponding to position weights in the binary system. If we drive the inputs of this circuit with digital gates so that each input is either 0 volts or full supply voltage, the output voltage will be an analog representation of the binary value of these three bits.

2) A R-2R Ladder:



A 4-bit R-2R Ladder DAC

The basic theory of the R-2R ladder network is that current flowing through any input resistor (2R) encounters two possible paths at the far end. The effective resistances of both paths are the same (also 2R), so the incoming current splits equally along both paths. The half-current that flows back towards lower orders of magnitude does not reach the op amp, and therefore has no effect on the output voltage. The half that takes the path towards the op amp along the ladder can affect the output. The inverting input of the op-amp is at virtual earth. Current flowing in the elements of the ladder network is therefore unaffected by switch positions.

If we label the bits (or inputs) bit 1 to bit N the output voltage caused by connecting a particular bit to Vr with all other bits grounded is:

Vout = Vr/2N

where N is the bit number. For bit 1, Vout =Vr/2, for bit 2, Vout = Vr/4 etc.

Since an R/2R ladder is a linear circuit, we can apply the principle of superposition to calculate Vout. The expected output voltage is calculated by summing the effect of all bits connected to Vr. For example, if bits 1 and 3 are connected to Vr with all other inputs grounded, the output voltage is calculated by:

Vout = (Vr/2)+(Vr/8)

which reduces to

Vout = 5Vr/8.

An R/2R ladder of 4 bits would have a full-scale output voltage of 1/2 +1/4 + 1/8 + 1/16 = 15Vr/16 or 0.9375 volts (if Vr=1 volt) while a 10bit R/2R ladder would have a full-scale output voltage of 0.99902 (if Vr=1 volt).

Performance Characteristics of DAC

The performance characteristics of a DAC include resolution, accuracy, linearity, monotonicity, and settling time:

- *Resolution*.

  The resolution of a DAC is the reciprocal of the number of discrete steps in the output. This, of course, is dependent on the number of input bits. For example, a 4-bit DAC has a resolution of one part in 2" - 1 (one part in fifteen).

  Expressed as a percentage, this is (1/15)100 = 6.67%. The total number of discrete steps equals 2" - 1, where *n* is the number of bits. Resolution can also be expressed as the number of bits that are converted.

- *Accuracy*.

  Accuracy is a comparison of the actual output of a DAC with the expected output. It is expressed as a percentage of a full-scale, or maximum, output voltage. For example, if a converter has a full-scale output of 10V and the accuracy is ±0.1 %, then the maximum error for any output voltage is (10 V) (0.001) =10 rnV. Ideally, the accuracy should be, at most, ±'/2 of an LSB. For an 8-bit converter, 1 LSB is 1/256 = 0.0039 (0.39% of full scale). The accuracy should be approximately ±0.2%,

- *Linearity*.

  A linear error is a deviation from the ideal straight-line output of a DAC. A special case is an offset error, which is the amount of output voltage when the input bits are all zeros.

- *Monotonicity*.

  A DAC is monotonic if it does not take any reverse steps when it is sequenced over its entire range of input bits.

- *Settling time*.

  Settling time is normally defined as the time it takes a DAC to settle within ±'/2 LSB of its final value when a change occurs in the input code.